REMARKS

Present Status of the Application

The Office Action dated June 14, 2006 rejected claims 1-19 under 35 USC 101, 35 USC 112, first paragraph, and 35 USC 112, second paragraph based on the asserted reasons as discussed below herein. New claims 20-26 have been added. The claims 20-26 are fully supported by the disclosure including the specification and the drawings; therefore, no new matter has been added.

Discussion of the claim rejections under 35 USC 101

Regarding the rejection of claims 1-19 under 35 U.S.C. 101 for the claimed invention is allegedly not supported by either a specific and substantial asserted utility, a credible utility, or a well established utility, the following are the traversal:

35 U.S.C. 101 recites the following: "Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title."

Excerpts from the present invention recite as follow:

[0005] In order **to rearrange and provide the received pixel data based on the requirement of different operation mode, a line buffer is commonly used in the LCD timing controller to cache the line pixel data, such that the line pixel data can be accurately transmitted by the timing controller. Wherein, in order to support the**

read and write operations simultaneously, a dual port memory is commonly used as the line buffer. However, the dual port memory occupies large space inside the integrated circuit (IC), thus it is hard to reduce the product cost and size.

[0006] Therefore, the **object** of the **present invention is to provide a method for accessing a single port memory.** In this method, **a single port memory is used as the line buffer in a display control circuitry or in a liquid crystal display system to fulfill the requirement of simultaneously reading and writing the line buffer.**

[0013] In summary, in the **method for accessing the single port memory in the present invention,** the single port line buffer is divided into N memory blocks, and different memory blocks in the line buffer are sequentially read out or written into based on the requirement of the normal mode or PLM mode operation. Therefore, **the single port memory can be used in the display control circuitry or in the liquid crystal display system as the line buffer, such that the requirement of simultaneously reading and writing the line buffer is achieved.**

[0031] Therefore, with the method for accessing the single port memory in the present invention, different memory blocks in the single port line buffer are accessed by turns based on the requirement of the PLM mode operation. **Accordingly, the single port memory can be used as the line buffer in the display control circuitry or in the liquid crystal display system, so as to fulfill the requirement of simultaneously reading and writing the line buffer without any clashing.**

Based upon the above recitations from paragraphs [0005], [0006], [0013], and [0031] of the present invention, the following are clearly found to support the "substantial and specific utility or credible asserted utility requirement" under 35 U.S.C. 101":

1) The utility of **present invention**: providing a new method for a single port memory to used as the line buffer in a display control circuitry to fulfill the requirement of simultaneously reading and writing the line buffer. And to fulfill the requirement of simultaneously reading and writing the line buffer without any clashing.

2) On the other hand, **conventional technology** teaches the following instead: a line buffer is used in the LCD timing controller to cache the line pixel data, to support the read and write operations simultaneously, a dual port memory is commonly used as the line buffer. However, the dual port memory occupies large space inside the integrated circuit (IC), thus it is hard to reduce the product cost and size. Based upon 1) and 2) above, it is easy to see that the "single port memory as line buffer" in the present invention vs. the "dual port memory as line buffer" in conventional technology clearly provides the "substantial and specific utility" for satisfying the requirements under 35 U.S.C. 101.

Discussion of the claim rejection under 35 USC 112, first paragraph

Regarding the assertion concering "not support any a specific of "a memory" or that claims do not "specific size of "a memory"", Claim 1 is amended as "providing a memory having N blocks" so as to overcome the above rejection.

Regarding the assertion concerning "receiving a plurality of line data" and lack of disclosure by the claims of what is used to receive line data and how to transfer data value to a memory, the following are the traversal:

35 U.S.C. 112 recites the following: " The specification shall contain a written description of the invention, and of the manner and process of making and using it, in

such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention...."

Based upon 35 U.S.C. 112, it is clear that the "specification" (as a whole) shall provide for the "disclosure" or "written description" function, and not the "claims" only as alluded to on page 2 of the Office Action for the aforementioned rejection.

Regarding "N integer" being asserted to not define being an odd or even number in claim 1, the claims are amended for clarity, such as, as in amended claim 1 recites: "....~~dividing~~ providing a memory ~~into~~having N memory blocks, wherein N is an positive integer; receiving a plurality of line data, and sequentially writing the line data into the ~~N~~memory blocks~~, wherein N is an integer~~".

Regarding lacking of support of writing and reading operation in claim 1, the traversal is the same as discussed previously, wherein basing upon 35 U.S.C. 112, it is clear that the "specification" (as a whole) shall provide for the "written description" function, and not the subject matter in claim 1 only as is implied in the above rejection; thus, writing and reading operation in claim 1 is fully supported in the entire disclosure including the specification and the drawings.

Regarding the asserted unclarity of claim 1 allegedly disclosed after writing more than N/2+1, read operation is started when however, claims 7, 13, and 16 is allegedly

disclosed that the reading step is started at after writing of N/2 + 2, the time to read at claim 1 is "after writing more than N/2+1 memory blocks", while the time to read at claims 3, 7, 13 and 16 is "after writing N/2+2 memory blocks." In other word, the time to read defined by claims 3, 7, 13 and 16 is within the time defined by claim 1, and thus no ambiguity or unclarity exits.

Regarding the rejection of claims 1-19 under 35 U.S.C. 112, first paragraph, because the claimed invention is allegedly not supported by either a specific and substantial asserted utility, a credible utility, or a well established utility, the corresponding traversal is the same as that of which was previously discussed in the Section under "Discussion of the claim rejections under 35 USC 101". As a result, the above rejection should be withdrawn.

Based upon the proper traversal for each item for the rejections discussed above, all of the corresponding claim rejections under 35 U.S.C. 112, first paragraph should be withdrawn.

Discussion of the claim rejection under 35 USC 112, second paragraph

Regarding the assertion that claims 1-19 recites the broad recitation "a memory, N of claim 16, and the claim also recites after writing more than N/2+1 memory blocks, starting to read in claim 1, but in claim 4 dependent from claim 1, the reading step started at N/2+1, these are invalid claims, an apparatus in claim 18-19..." on page 4 of the Office Action, claim 4 is amended for clarity, and is recited as follows:

"....wherein the reading step ~~is started~~ firstly reads the from the ~~memory blocks which are written in a sequence of~~ the 1st memory block and the ~~(N/2+1)~~xth memory block"

The amended claim 4 clearly describes "the reading step firstly reads from the the 1st memory block and the (N/2+1)th memory block" for the sake of clarity. Claim 4 therefore does not describe the time to read, which was misunderstood as discussed on page 4 of the Office Action. As a result, the above rejection should be withdrawn.

Regarding the assertion that claims do not specify, which is an apparatus, is used to perform the method in claim 19, and that only a single port memory cannot use to anything in a memory device, claim 19 is canceled, thus rendering the above rejection moot.

Regarding the assertion that an apparatus claim cannot dependent from a method claim, according to MPEP 2113, product-by-process claims are perfectly valid claims, furthermore, claims 18 and 19 are canceled, rendering the rejection to claims 18-19 moot.

Regarding the assertion that claims 18-19 contain not enough information of an apparatus to use to read or write a memory device, and the assertion that Applicant disclosed no drawing to show an apparatus uses to read or writing operations in device, claims 18 and 19 are canceled, rendering the rejection to claims 18-19 moot.

Based upon the proper traversal for each item for the rejections discussed above, all of the corresponding claim rejections under 35 U.S.C. 112, second paragraph should be withdrawn.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-6, 10-13, 16-17, and 20-26 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted

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